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OPTICALLY INTRACONNECTED COMPUTER EMPLOYING DYNAMICALLY RECONFIGURABLE HOLOGRAPHIC OPTICAL ELEMENT

Origin of the Invention:

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

Background of the Invention:

The present invention relates to digital computer architectures and internal communications thereof and, more particularly, to an optically intraconnected computer comprising, a memory for holding a sequence of instructions to be executed; logic for accessing the instructions in sequence; logic for determining for each instruction the function to be performed and the effective address thereof; a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing the instructions; and, element selection logic connected to the logic determining the function to be performed for each instruction for determining the class of each function and for causing the instruction to be executed by those elements which perform the associated logical sequences affecting the instruction execution in an optimum manner; wherein, the element selection logic includes means for transmitting and switching signals to the elements optically comprising, a holographic optical element including a holographic reflective surface mounted adjacent and parallel to the common support substrate; a plurality of light source means carried by the common support substrate for directing signal-modified light beams towards the holographic reflective surface to be reflected thereby back towards the common support substrate; and, a plurality of light

detecting means carried by the common support substrate and operably connected to respective ones of the elements to provide electrical signals thereto for detecting selected ones of the light beams as reflected by the holographic reflective surface and providing associated electrical signals derived from the reflected light beams.

In its simplest description, a digital computer is a device which executes a series of instructions relative to a set of data to accomplish a result. A very basic prior art digital computer is generally indicated as 10 in Figure 1. The computer 10 has a memory 12 containing instructions and data and an arithmetic and logic unit (ALU) 14 connected to a clock 16. The ALU 14 includes registers and logic to repetitively perform the functions shown in Figure 2. As part of performing its computing functions, the ALU 14 can read from and write to the memory 12 on an individually addressable basis; that is, the memory 12 comprises a matrix of individually addressable locations containing binary (digital) information which can be employed as either an instruction or a piece of data by the ALU 14. The operation of the ALU 14 and its accesses to the memory 12 are controlled by the clock 16 in that the pulses of the clock 16 determine the points in time when the functional elements of the ALU 14 can perform and the memory 12 can be read from and written to.

As depicted by Figure 2, the ALU 14 sequentially fetches the next instruction to be executed from the memory 12. The instruction is then inspected to determine the function to be performed (i.e. add, multiply, etc.) and the effective address of the data (i.e. one of the registers, a location in memory 12, etc.). The ALU 14 then performs the indicated function employing pre-established hardware instruction performance logic 18.

As can be appreciated, the design and construction of a "new" digital computer operating as above was a time consuming task. As vacuum tubes gave way to discrete component transistors, and the like, and then to integrated

circuits; and, as the evolutionary period between new integrated circuits and the technology of producing them became less and less, the designing and implementing of the pre-established hardware instruction performance logic 18 as described above became more and more impractical. Microprocessor design traditionally involves much combinational (random) custom logic in the layout of the ALU. In such an implementation, the basic instruction set of the central processing unit (CPU) which executes the CPU's instruction set is embedded in difficult-to-modify logic which is not programmable, being embodied in immutable hardware. This approach suffers from unpredictable logic errors, delays caused by the impedance of the conductors, and requires excessive space on the CPU's chip. Thus, the instruction execution rate -- and the clock speed -- are degraded significantly from that attainable by the CPU.

Attempts to make programmable instruction sets have resulted in the development of micro-coded CPUs operating as depicted in Figure 3. Whereas the basic instructional fetching and evaluation procedure of prior computers is retained, a micro-coded CPU's hardware-implemented instructions are minimized to a set of "standard" operations which can be performed in various combinations to accomplish more complex "instructions". The instruction definitions are embodied in sequences of "micro-code" instructions or firmware 20 typically contained in erasable programmable read only memory (EPROM) 22. The EPROM memory 22 may be erased by flooding with ultraviolet light, or electrically (EEPROMS). This family of machines is easily modified, but also suffers similar speed degradation. Moreover, while "easily" modifiable to a new configuration, such modification is a bench top undertaking and is not adaptable to on-line and/or real-time reconfiguration.

In one approach to the residual problems of micro-coded computers, reduced instruction set computers (RISC) have been designed. They are compact and fast, but can only be customized for a limited group of operations.

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Statement of the Invention:

This invention provides a new computer architecture family which is fast, compact, easily reconfigurable, and, in some cases, even dynamically reconfigurable as to its performed instruction definitions.

The foregoing is accomplished in a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction the function to be performed and the effective address thereof, and logic for executing each instruction, by the improvement of the present invention comprising, the logic for executing instructions comprising a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing instructions; and, element selection logic connected to the logic determining the function to be performed for each instruction for determining the class of each function and for causing the instruction to be executed by those elements which perform the associated logical sequences affecting the instruction execution in an optimum manner.

In the preferred embodiment, the element selection logic includes means for accepting dynamic inputs designating changes in the operating environment of the computer and means for changing the ones of the elements which execute each instruction whereby instruction execution is affected in an optimum manner for the present dynamic conditions.

Optionally, the elements can comprise individual arithmetic and logic units contained on a single central processor unit chip; or, the elements can comprise individual reduced instruction set computers contained on a single central processor unit chip.

Further in the preferred embodiment, the element selection logic portion for causing the instruction to be executed by the elements which perform those associated

logical sequences affecting the instruction execution in an optimum manner includes means for transmitting and switching signals to the elements optically.

The preferred means for transmitting and switching signals to the elements optically comprises, a holographic optical element including a holographic reflective surface mounted adjacent and parallel to the common support substrate; a plurality of light source means carried by the common support substrate for directing signal-modified light beams towards the holographic reflective surface to be reflected thereby back towards the common support substrate; and, a plurality of light detecting means carried by the common support substrate and operably connected to respective ones of the elements to provide electrical signals thereto for detecting selected ones of the light beams as reflected by the holographic reflective surface and providing associated electrical signals derived from the reflected light beams.

In one embodiment, there are means for switching the light source means on and off to determine which ones of the light detecting means received the reflected light beams whereby the sequence of the elements receiving and processing the signals is determined.

In the preferred embodiment, light modulation means are disposed between the light source means and the light detecting means for selectively blocking and passing the light beams whereby the sequence of the elements receiving and processing the signals is determined.

The preferred light modulation means is a novel reconfigurable holographic optical element including a holographic reflective surface mounted adjacent and parallel to the common support substrate and light modulation means disposed adjacent the holographic reflective surface for selectively blocking and passing light beams from reflecting from the holographic reflective surface at individual pixel positions thereof; and, means for switching the light modulation means on and off at the individual pixel

positions thereof to determine which ones of the light detecting means receive the reflected light beams whereby the sequence of the elements receiving and processing the signals is determined.

List of Cited References:

A device called a holographic optical element (HOE) is incorporated into several of the embodiments of the present invention and forms the heart of the preferred embodiments thereof. The HOE and its use in conjunction with VLSI is described in great detail in the following publications, of which copies are being filed contemporaneously herewith:

1. HOLOGRAPHIC OPTICAL INTERCONNECTS FOR VLSI by L.A. Bergman, et al. as reprinted from "Optical Engineering" 25(10), 1109-1118 (October 1986).

2. IMPLEMENTATION OF OPTICAL INTERCONNECTIONS FOR VLSI by L.A. Bergman, et al. as reprinted from "IEEE Transactions on Electron Devices", Vol. ED-34, No. 3, (March 1987).

3. APPLICATIONS AND DESIGN CONSIDERATIONS FOR OPTICAL INTERCONNECTS IN VLSI by L.A. Bergman, et al. as reprinted from "SPIE", Vol. 625, 117-126 (1986).

Discussion of the Cited References:

The HOE device as described in the above-referenced articles is incorporated into various embodiments of the present invention and a novel variation is disclosed herein as part of the present invention. The above-referenced articles do not show or suggest the use of a HOE as in the present invention or the novel variation of a HOE (i.e. a dynamically reconfigurable HOE) as is part of this this invention.

Brief Description of the Drawings:

Figure 1 is a simplified block diagram of a basic prior art computer architecture.

Figure 2 is a functional block diagram of the operation of the computer architecture of Figure 1.

Figure 3 is a functional block diagram of the operation of another prior art computer architecture of the microcode executing variety.

Figure 4 is a simplified side view of a HOE being used to broadcast signals from one part of an adjacent computer chip to other parts of the chip optically.

Figure 5 is a semi-functional block diagram of a computer architecture according to the present invention in a basic embodiment thereof not employing a HOE therein.

Figure 6 is a semi-functional block diagram of a computer architecture according to the present invention in a basic embodiment thereof employing a prior art HOE therein.

Figure 7 is a semi-functional block diagram of a computer architecture according to the present invention in a semi-preferred embodiment thereof employing a reconfigurable HOE of the present invention therein.

Figures 8(a)-8(d) are simplified side views of a HOE being used to transmit signals from one part of an adjacent computer chip to another part of the chip optically in the manner of Figure 4 and showing the difference in the passive operation of a prior art HOE and active operation of a dynamically reconfigurable HOE according to the present invention.

Figure 9 is a simplified side view in the manner of Figures 4 and 8 of the dynamically reconfigurable HOE of the present invention being used to control the transmission of signals from one part of an adjacent computer chip to another part of the chip optically.

Figure 10 is a perspective representation of the manner of operation of the reconfigurable HOE of the present invention as shown in Figure 9.

Figure 11 is a semi-functional block diagram of a computer architecture according to the present invention in its preferred embodiment employing a reconfigurable HOE of

the present invention therein responding to both internal and external influences in the dynamic reconfiguration of the HOE.

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Detailed Description of the Invention:

Prior to an actual description of the various computer architectures which form the family of the present invention, brief mention should be made of the HOE device employed therein. While those interested can get detailed information about HOEs and their use from the above-referenced articles, the aspects thereof of particular interest to the present invention are shown in simplified form in Figure 4. Basically, the HOE 24 can be thought of as an optical switching surface. The chip 26 and HOE 24 are physically juxtaposed in parallel spaced relationship to one another. The chip 26 contains one or more sources 28 of a laser beam 30 which is directed towards the surface of the HOE 24. The laser beam(s) 30 are reflected by the holographic surface of the HOE 24 back towards the chip 26 to be detected by one or more optical detectors 32 wherein an electrical signal is created for further use by the logic of the chip 26. Thus, signal transmissions can be made at light speed without the delays, and the like, associated with electrically conductive paths. Moreover "broadcast" transmissions can be made to multiple points simultaneously and the problems of complex interconnection layout between points on the chip 26 are eliminated. Again, this procedure and the physiology required therefor are described in detail in the above-listed documents provided herewith.

Turning now to Figure 5, a basic implementation of the present invention is shown in simplified form. In essence, the computer of Figure 5 operates in the manner of the prior art computer of Figure 2; that is, the function performance is accomplished by hardware instruction logic. In this embodiment of the present invention, however, the hardware instruction logic is contained in individualized RISC processors 34 contained on the CPU chip 36. Each of the

RISC processors 34 is configured to perform an optimized instruction set. When the next instruction to perform has been fetched from memory 12, its function class is determined and input to processor selection logic 38, which determines which of the RISC processors 34 is best suited (i.e. specifically designed) to perform that function. In the preferred embodiment, the processor selection logic 38 also responds to dynamic inputs at 40 whereby the selection of the RISC processor(s) 34 can be modified as a function of changing dynamic conditions. It should be noted in this regard that the embodiment of Figure 5 is different from a multi-processor computer architecture wherein functional sequences of instructions or "programs" are assigned to different ones of interconnected computers (CPUs) for execution. In this embodiment of the present invention, the execution of each instruction in sequence is selectably and switchably accomplished by an appropriate RISC processor 34 contained within a single CPU 36.

The functional operation of another embodiment of the present invention is shown in Figure 6 wherein multiple RISC processors 34 are again employed and a HOE 24 is employed in its switching capacity to cause performance, in each case, through an optical interface by the RISC processor 34 best suited to the circumstances at the time. The HOE 24 is controlled by the switching logic 42 which controls which of the laser beams 30 from the light source selector 44 are directed to the reflecting surface of the HOE 24 to be reflected thereby to the desired RISC processor 34. The switching logic 42 is, in turn, basically controlled by the logic at 46 which determines the function to perform and its functional class; but, preferably, can be controlled as well by dynamic inputs 42 responding to changed conditions as in the prior embodiment. Both this embodiment and the prior embodiment of Figure 5 can be totally hardware oriented; or, if desired, either embodiment can be operated as a micro-coded computer by having the RISC processors access microcode firmware 20 as depicted in Figure 6.

In the semi-preferred embodiment of the present invention shown in the functional block diagram of Figure 7, the firmware/semi-software instruction sets of the prior embodiments are eliminated along with their physical interconnections and the problems associated therewith. The "micro-code" is embodied within the holographic surface of the the reconfigurable HOE 48 and is "executed" by sequentially directing the laser beam containing the execution data from one area of the juxtaposed CPU chip 36 to another.

Before continuing to the preferred embodiment of the present invention, it is necessary to digress briefly to the drawings of Figures 8-10 wherein a novel dynamically reconfigurable HOE 48, as is part of the present invention and necessary thereto, is shown and distinguished over the basic HOE 24 in simplified form. The reconfigurable HOE 48 comprises a basic HOE 24' having a spatial light modulator (SLM) 50 disposed over (or as part of) the holographic reflective surface of the HOE 24' facing the chip 26'. The spatial light modulator 50 (or light valve) is a device presently known in the art by which each pixel position of a two-dimensional matrix can be individually modified as to its light passage qualities through electrical, magnetic, or other, means. A common example of such devices is familiar from so-called "liquid crystal" displays as employed in wristwatches, and the like. As with the HOE itself, the spatial light modulator art is a dynamic art changing and improving daily and those interested in the specifics of the latest developments in that art are directed to the literature generally available. In the interest of simplicity and the avoidance of redundancy, details of spatial light modulators and their operation will be omitted herein. It is sufficient to say for purposes of the present invention that, either as a replacement for or in addition to the holographic surface of the HOE 24', the dynamically changable SLM 50 can be changed under the control of reconfiguration inputs at 52 to, in turn, change the

switching sequence of the HOE 24'. It should also be noted that while the spatial light modulation takes place on or directly adjacent to the holographic reflective surface of the HOE in the example depicted and described herein, as those skilled in the art will recognize and appreciate, the SLM could be interposed in the path of the light beam at a distance and its operation affected through the use of focusing optics well known in the art. While not preferred, a device operating as what could be referred to as a transmitting HOE (i.e. a form of pixel-oriented, matrix, spatial light modulator), as is known in the art, could also be employed in place of a reflective HOE. Also, the reflective surface of the HOE could comprise a plurality of reflective angles instead of a holographic surface, per se, within the scope and spirit of the present invention.

The difference in operation between a prior art HOE 24 as employed in the present invention in the embodiment of Figure 6 and the novel reconfigurable HOE 48 employed in the preferred embodiments can be understood best with reference to Figures 8(a) through 8(d). Figures 8(a) and 8(b) show the operation of a standard HOE 24. To communicate with detector "A", the laser beam 30 from laser source "A" is turned on and reflected from the holographic reflective surface of the HOE 24 at point "A" as depicted in Figure 8(a). To communicate with detector "B", on the other hand, the laser beam 30 from laser source "B" is turned on and reflected from the holographic reflective surface of the HOE 24 at point "B" as depicted in Figure 8(b). Thus, since the HOE 24 is a passive device, switching through its use can only be accomplished through the control of the source(s) 28 of the laser beam(s) 30.

By contrast, as depicted in Figures 8(c) and 8(d), the reconfigurable HOE 48 is a dynamic or active device. Multiple laser beams 30 from multiple sources 28 can be directed at the reflective holographic surface of the HOE 24' continually. Switching is accomplished by controlling the light passing qualities of the pixel positions of the

SLM 50. For example, as shown in Figure 8(c), To communicate with detector "A", the laser beam 30 from laser source "A" is allowed to reflect from the holographic reflective surface of the HOE 24 at point "A" while the pixel 54 of the SLM 48 at point "B" is darkened to prevent the laser beam 30 from source "B" to pass through and be reflected. To communicate with detector "B", on the other hand, the pixels 54 are reversed so that the laser beam 30 from laser source "B" is reflected from the holographic reflective surface of the HOE 24 at point "B" and the laser beam 30 from laser source "A" is blocked, as depicted in Figure 8(d).

Turning now to Figure 11 in combination with Figure 10, the preferred embodiment of the present invention will now be described functionally. In this embodiment, the instruction sets are physically removed from the CPU and instructions are to one or more ALUs (as appropriate) via light signals, with input and output signals routed point-to-point by the reconfigurable HOE 48 under the control of the reconfiguration logic 56 with inputs from the logic determining the function and class 46 as well as dynamic inputs 40. The light signals are preferably generated by laser diodes and received by photodiodes as described in the above-referenced literature. Functionally, this embodiment may be envisioned as several RISC designs overlaid on a common VLSI substrate with each RISC being designed specifically for a specific operation such as Boolean operations, control, convolution, and the like in the manner previously described with respect to Figures 5-7. Each subset of instructions is mapped onto one of the ALUs by the HOE 50, the specific subset desired being switched by turning on one set of laser diodes while switching off all the other sets, and/or by electronically selecting signals to be sent via a single set of laser diodes, etc. Thus, instruction set changes may be made fairly rapidly. In basic form, the foregoing description also applies to the embodiment of Figure 7 as previously discussed. In this

embodiment, however, in addition to having multiple ALUs on the CPU portion of the chip so as to take advantage of specialized "hardware" capabilities in each case as appropriate, the HOE 48 itself is dynamically reprogramable by the reconfiguration logic 56 in response to dynamic inputs at 40. As a result, changes can be made very rapidly; in fact, it is contemplated that, possibly, changes will be able to be affected at clock speed.

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